In The Drawings

Submitted herewith are proposed drawing corrections to Figure 6 marked in red.

In The Claims

Please cancel without prejudice or disclaimer claim 22.

Please add new claims 26-41.

26. (Newly Added) A method for arranging bump pads on a surface of an integrated circuit die, comprising the steps of:

providing a first signal bump pad;

connecting a first end of a first trace to said first signal bump pad;

connecting a second end of said first trace to a first input/output cell, wherein said first trace radiates in a first direction;

providing a second signal bump pad;

connecting a first end of a second trace to said second signal bump pad;

connecting a second end of said second trace to a second input/output cell, said second trace radiates in a second direction, and said first direction is opposite said second direction;

disposing said first trace and said second trace on opposite sides of a first line defined by said first signal bump pad and said second signal bump pad;

providing a first power bump pad having a third trace radiating in said first direction and connecting to a first power bus;

providing a second power bump pad having a fourth trace radiating in said second direction and connecting to a second power bus, said third trace and said fourth trace disposed on opposite sides of a second line defined by said first power bump pad and said second power bump pad;

disposing said first signal bump pad closer to a center of said integrated circuit die than said first power bump pad; and

disposing said second signal bump pad closer to said center of said integrated circuit die than said second power bump pad.

27. (Newly Added) The method of claim 26 further comprising the step of providing a core power region located centrally on said integrated circuit die, said step of providing said core power region comprising the steps of:

providing a first power rail;

providing a second power rail;

providing a first plurality of power bump pads of a first type and coupling to said first power rail;

providing a second plurality of power bump pads of a second type and coupling to said second power rail; and

disposing said first plurality of power bump pads of said first type and said second plurality of power bump pads of said second type in an alternating manner between said first power rail and second power rail.

28. (Newly Added) The method of claim 27 further comprising the step of arranging said first and second lines substantially coincident with each other.

29. (Newly Added) The method of claim 28 further comprising the step of arranging said first and second directions substantially opposite to each other.

30. (Newly Added) The method of claim 29 wherein said first type is a power supply and said second type is a ground.

31. (Newly Added) A method for distributing pads on a surface of a semiconductor die, said method comprising the steps of:

calculating a power-signal ratio;

establishing a number N of I/O bump pads to be allocated per pair of power bump pads based on the power-signal ratio;

arranging said N I/O bump pads and pair of said power bump pads linearly and repeating said linear arrangement within four edge groups on said surface of said die;

identifying four corner regions, one corner region in each corner of the die surface; and

arranging a core power group within a center of said edge groups and said corner regions.

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~~32.~~ (Newly Added) The method of claim ~~31~~ wherein said N I/O bump pads and pair of said power bump pads are arranged in a column and are replicated across an edge of said die in said edge groups.

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~~33.~~ (Newly Added) The method of claim ~~31~~ wherein said identifying said corner regions comprises the steps of:

establishing a corner region size based on the ratio of said N I/O bump pads to said power bump pads;

designating a first bump pad row;

setting a counter M to one:

designing an M+1 sector by designating as many bump pads as may be located within a leftmost column to belong to said M+1 sector;

designing an M+2 sector by designating as many bump pads as may be located within a topmost row to belong to said M+2 sector;

filling the remainder of said M+1 sector by designating bump pads within the top of a leftmost remaining column to belong to said M+1 sector;

filing the remainder of said M+2 sector by designating bump pads on the left of a topmost remaining row to belong to said M+2 sector;

evaluating whether said M+1 and said M+2 sectors are complete, and if the sector is incomplete, repeating said M+1 filling step and said M+2 filling step until said sectors are complete;

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incrementing the counter to M+2;

deciding whether more than one sector remains, and repeating said M+1 sector design step and all subsequent steps when one more than one sector remains until one or less sectors remain; and

determining whether one sector remains and if one sector remains designating all remaining undesignated bump pads to the final sector.

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~~34.~~ (Newly Added) The method of claim ~~33~~ further comprising the step of designating two bump pads in each sector closest to an edge of the die as power bump pads, wherein said two bump pad designating step is subsequent to said one sector remaining determining step.

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~~35.~~ (Newly Added) The method of claim ~~34~~ further comprising the step of providing balanced connections between said bump pads and a power ring and a plurality of I/O cells located near the edge of said die.

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~~36.~~ (Newly Added) A method for arranging bump pads on a surface of an integrated circuit die, comprising the steps of:

providing a first power bus on said surface of said integrated circuit die;

providing a second power bus on said surface of said integrated circuit die;

providing a first bump pad having a first trace radiating in a first direction;

connecting said first trace to a first input/output cell;

providing a second signal bump pad having a second trace radiating in a second direction different from the first direction;

connecting said second trace to a second input/output cell;

disposing said first trace and said second trace on opposite sides of a first line defined by said first signal bump pad and said second signal bump pad;

providing a third signal bump pad having a third trace radiating in said first direction;

connecting said third trace to a third input/output cell;

providing a fourth signal bump pad having a fourth trace radiating in said second direction;

connecting said fourth trace to a fourth input/output cell;

disposing said third trace and said fourth trace on opposite sides of a second line defined by said third signal bump and said fourth signal bump;

providing a first power bump pad and connecting to said first power bus;

providing a second power bump pad and connecting to said second power bus;

disposing said first and second signal bump pads on an opposite side of said first power bus from said third and fourth signal bumps;

disposing said first signal bump pad farther from said first power than said second signal bump pad; and

disposing said fourth signal bump pad farther from said first power bus than said third signal bump pad.

37. (Newly Added) The method of claim 36 further comprising the steps of:

providing a first power rail;

providing a second power rail;

coupling a first plurality of power bump pads of a first type to said first power rail;

coupling a second plurality of power bump pads of a second type to said second power rail; and

disposing said first plurality of power bump pads of said first type and said second plurality of power bump pads of said second type in an alternating fashion between said first power rail and second power rail.

38. (Newly Added) The method of claim 37 further comprising the step of arranging said first and second lines substantially coincident with each other.

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~~39.~~ (Newly Added) The method of claim ~~38~~ further comprising the step of arranging said first and second directions substantially opposite to each other.

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~~40.~~ (Newly Added) The method of claim ~~39~~ wherein said first type is a power supply and said second type is a ground.

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~~41.~~ (Newly Added) A method for arranging bump pads on a surface of a flip-chip die, comprising the steps of:

providing at least one power bump;

linearly aligning a plurality of input/output bumps, wherein said linearly aligned plurality of input/output bumps are aligned with said at least one power bump;

positioning said at least one power bump intermediate among said linearly aligned plurality of input/output bumps;

forming said at least one power bump and said linearly aligned plurality of input/output bumps in an array; and

replicating said array linearly across said flip-chip die, thereby forming a linear bump array arrangement.

REMARKS

Discussion of Drawing

Minor errors were noted in Figure 6 of the drawings in that the Vdd voltage bump and Vss ground bump are not respectively indicated as elements 605 and 606 (see specification, page 14, line 23-25). Accordingly, Figure 6 is submitted herein by amendment to include "605" and "606".

Discussion of Claims

In the Office Action, claims 23-25 stand allowable over the prior art of record.

In the Office Action, claim 22 stands rejected 35 U.S.C. 102 as allegedly being anticipated by Seefeldt et al. (U.S. Patent No. 4,978,633).